CLAIMS

1. A common mode signal suppressing circuit for suppressing common mode signals propagating with identical phases through two conductor lines, the common mode signal suppressing circuit comprising:

a first winding inserted to one of the conductor lines at a specific first point;

a second winding that is inserted to the other of the conductor lines at a second point corresponding to the first point and is coupled to the first winding, the second winding suppressing the common mode signals in cooperation with the first winding;

a third winding coupled to the first and second windings such that a mutual inductance is generated between the third winding and the first and second windings; and

a phase-inverted signal transmitting means connected to the third winding and to the one of the conductor lines at a third point different from the first point, the transmitting means being further connected to the other of the conductor lines at a fourth point corresponding to the third point and different from the second point, the transmitting means transmitting a phase-inverted signal for suppressing the common mode signals, wherein:

when a source of the common mode signals is located at a point closer to the third and fourth points than the first and second points except a point between the first and third points and a point between the second and fourth points, the transmitting means detects a common mode signal and supplies the phase-inverted signal to the third winding, the phase-inverted signal having a phase opposite to a phase of the common mode signal detected, and the third winding injects the phase-inverted signal to the two conductor lines

through the first and second windings; and

when the source of the common mode signals is located at a point closer to the first and second points than the third and fourth points except a point between the first and third points and a point between the second and fourth points, the third winding detects a common mode signal, and the transmitting means injects the phase-inverted signal to the two conductor lines, the phase-inverted signal having a phase opposite to a phase of the common mode signal detected by the third winding.

2. The common mode signal suppressing circuit according to claim 1, further comprising an impedance element provided on the two conductor lines at a point between the first and third points and a point between the second and fourth points, the impedance element reducing a peak value of a common mode signal passing therethrough.

3. The common mode signal suppressing circuit according to claim 1, wherein the phase-inverted signal transmitting means incorporates a high-pass filter for allowing a common mode signal to pass therethrough.

4. The common mode signal suppressing circuit according to claim 3, wherein the high-pass filter incorporates a capacitor.

5. The common mode signal suppressing circuit according to claim 1, wherein the impedance element incorporates: a fourth winding inserted to one of the conductor lines; and a fifth winding that is inserted to the other of the conductor lines and coupled to the fourth winding and that suppresses

the common mode signals in cooperation with the fourth winding.

6. The common mode signal suppressing circuit according to claim 5, wherein each of the fourth and fifth windings has an inductance of 0.3 μH or greater.

7. The common mode signal suppressing circuit according to claim 1, wherein a coupling coefficient between the third winding and the first and second windings is 0.7 or greater.

8. A normal mode signal suppressing circuit for suppressing normal mode signals transmitted by two conductor lines and creating a potential difference between the two conductor lines, the normal mode signal suppressing circuit comprising:

a first inductance element inserted to one of the conductor lines at a specific first point;

a second inductance element coupled to the first inductance element such that a mutual inductance is generated between the first and second inductance elements;

a phase-inverted signal transmitting means connected to the second inductance element and to the one of the conductor lines at a second point different from the first point, the transmitting means transmitting a phase-inverted signal for suppressing the normal mode signals; and

an impedance element provided on the one of the conductor lines at a point between the first and second points, the impedance element reducing a peak value of a normal mode signal passing therethrough, wherein:

when a source of the normal mode signals is located at a point closer to the second point than the first point except a point between the first and second points, the transmitting means detects a normal mode signal and supplies the phase-inverted signal to the second inductance element, the phase-inverted signal having a phase opposite to a phase of the normal mode signal detected, and the second inductance element injects the phase-inverted signal to the one of the conductor lines through the first inductance element; and

when the source of the normal mode signals is located at a point closer to the first point than the second point except a point between the first and second points, the second inductance element detects a normal mode signal, and the transmitting means injects the phase-inverted signal to the one of the conductor lines, the phase-inverted signal having a phase opposite to a phase of the normal mode signal detected by the second inductance element.

9. The normal mode signal suppressing circuit according to claim 8, wherein the phase-inverted signal transmitting means incorporates a high-pass filter for allowing a normal mode signal to pass therethrough.

10. The normal mode signal suppressing circuit according to claim 9, wherein the high-pass filter incorporates a capacitor.

11. The normal mode signal suppressing circuit according to claim 9, wherein the high-pass filter incorporates a plurality of capacitors that are combined.

12. The normal mode signal suppressing circuit according to claim 8, wherein the impedance element incorporates a third inductance element inserted to the one of the conductor lines.

13. The normal mode signal suppressing circuit according to claim 12, wherein the third inductance element has an inductance of 0.3 μH or greater.

14. The normal mode signal suppressing circuit according to claim 8, wherein a coupling coefficient between the first and second inductance elements is 0.7 or greater.